MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2016/2017

EEN1046 – ELECTRONICS III

(All sections / Groups)

1 JUNE 2017
9.00 a.m. – 11.00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 7 pages with 4 Questions only excluding cover page.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.

Question 1 Apply the basic ideal op-amp circuit specifications to determine

(a) The output voltage V_0 in the circuit of Fig.Q1(a)

[4 Marks]

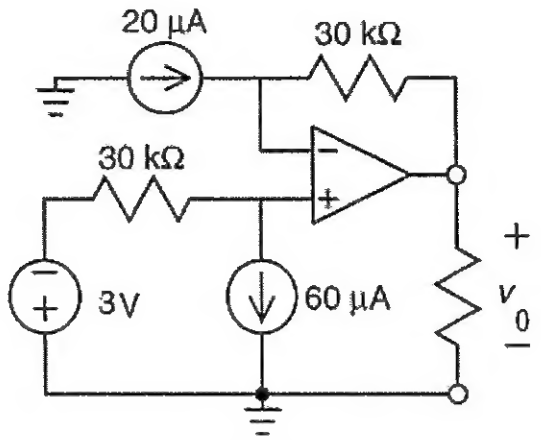

Fig.Q1(a)

(b) The current i in the circuit of Fig.Q1(b). Take R1=8kΩ, R2=2kΩ, Rf=2kΩ and R3=1kΩ

[5 Marks]

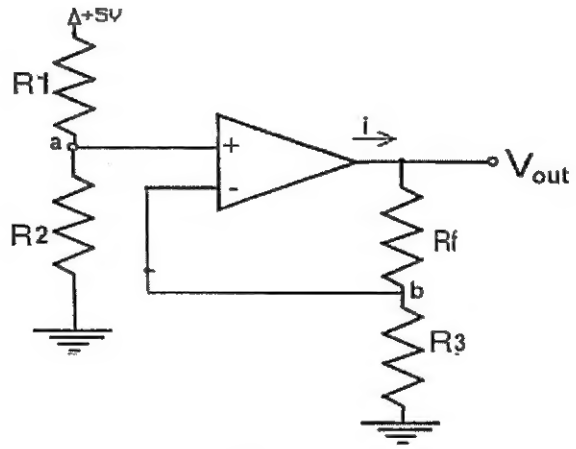

Fig.Q1(b)

(c) Currents I1, I2 and I3 in the circuit of Fig. Q1(c). Take, R1=1kΩ, R2=10kΩ, R3=20kΩ and R=1kΩ. Also assume breakdown voltage of Zener diode is equal to 1.2V.

[8 Marks]

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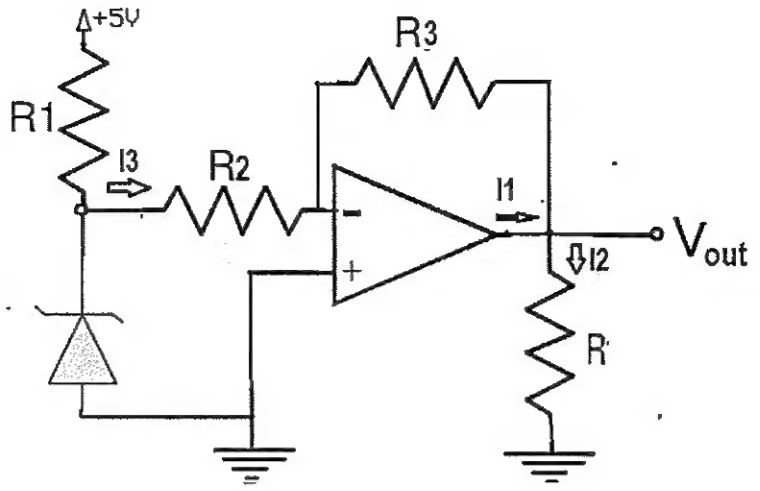

Fig.Q1(c)

(d) Output voltage V_{out} in the circuit of Figure Q1(iv). Assume $v_{in}(t)=10\cos(100t)$. Take $R_1=10\ \Omega$, $R_2=100\ \Omega$, L=10 mH and C=10μF.

[8 marks]

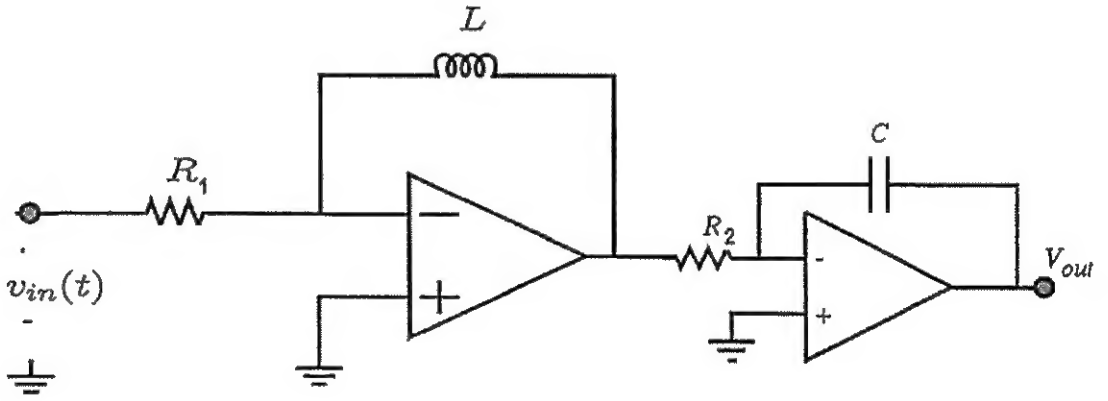

Fig.Q1(iv)

Continued .....

Question 2

(a) A student has analysed a practical op-amp which is wired in inverting configuration with grounded input and measured the output voltage 0.5V. Take R_f=100kΩ and R_I=10KΩ.

(i) Determine the input offset voltage

(ii) Sketch the circuit to mitigate the offset voltage

(iii) What are the sources to produce error voltage in practical op-amp?

(iv) Compare the offset voltage of part (i) with ideal op-amp.

[2+3+2+1 marks]

(b) A triangular wave of 20V peak-to-peak amplitude is applied to a practical op-amp whose slew rate is 10V/μs. For a sinusoidal wave of same frequency as triangular wave, determine the maximum amplitude of output signal that remain undistorted.

[6 marks]

(c) A student has recorded 1.2 V at the output of an op-amp whose differential gain is 10^4 for inputs of 90μV and 110μV respectively at the inverting and non-inverting terminals. Calculate

(i) The common mode signal gain

(ii) The CMRR of the amplifier

(iii) Express the CMRR in dB

(iv) Compare CMRR calculated in part (ii) with ideal op-amp value with proper explanation

[3+1.5+1.5+2 marks]

(d) An op-amp with unity gain bandwidth of 2MHz, slew rate of 1V/μs and output saturation voltage of 10V is used to design a non-inverting amplifier with gain of 10. If the input signal is sine wave of 25V peak-to-peak amplitude, determine the useful frequency range.

[3 marks]

Continued .....

Question 3

(a) A series voltage regulator circuit is as shown in Fig Q3 (a). Explain briefly about the following:

(i) The role of Zener diode in the circuit

[1 marks]

(ii) The effect on output voltage of the circuit due to change in input voltage V.

[3 marks]

(iii) The effect on output voltage of the circuit due to change in load resistance value.

[4 marks]

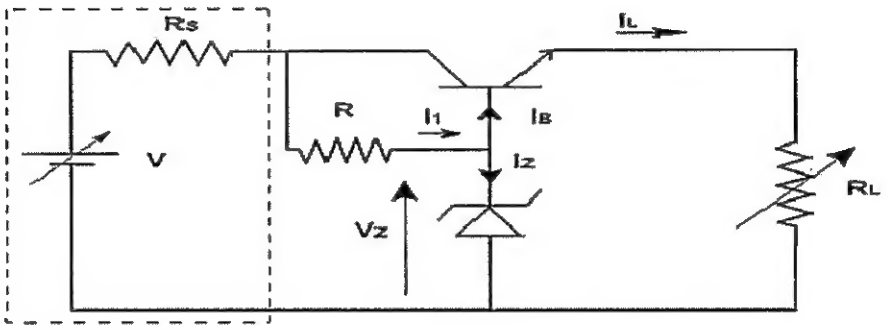

Fig. Q3 (a)

(b)

(i) The main drawback of any series regulator is the fact that if the load is shorted, the excessive load current can destroy the pass transistor. Draw a current limiter circuit for a current limit of 1A using diodes to protect a power supply from the possibility of damage due to overload.

[5 marks]

(ii) What is the main function of SCR (Silicon Controlled Rectifier) in over-voltage protection circuit?

[2 marks]

(c)

(i) Design a Wien Bridge Oscillator circuit, as shown in Fig. Q3 (c) to generate a sinusoidal waveform of 6 KHz at the output. Assume C=1nF, $R_1 = 2k\Omega$ and an ideal op-amp.

[6 marks]

Continued .....

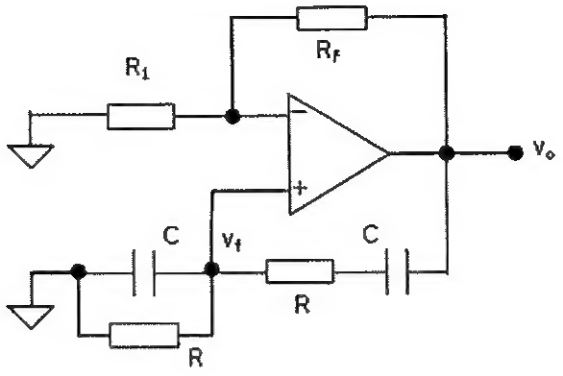

Fig. Q3(c)

(ii) Determine the maximum and minimum frequency of oscillations of the Wien Bridge Oscillator circuit having a resistor of 10 kΩ and a variable capacitor of 1nF to 100nF.

[4 marks]

Continued .....

Question 4

(a)

(i) What are the disadvantages of a simple comparator and how it can be avoided? Explain with a suitable circuit.

[5 marks]

(ii) Design the Schmitt trigger circuit as shown in Fig. 4 (a). Hysteresis voltage for the circuit is 8V.

[4 marks]

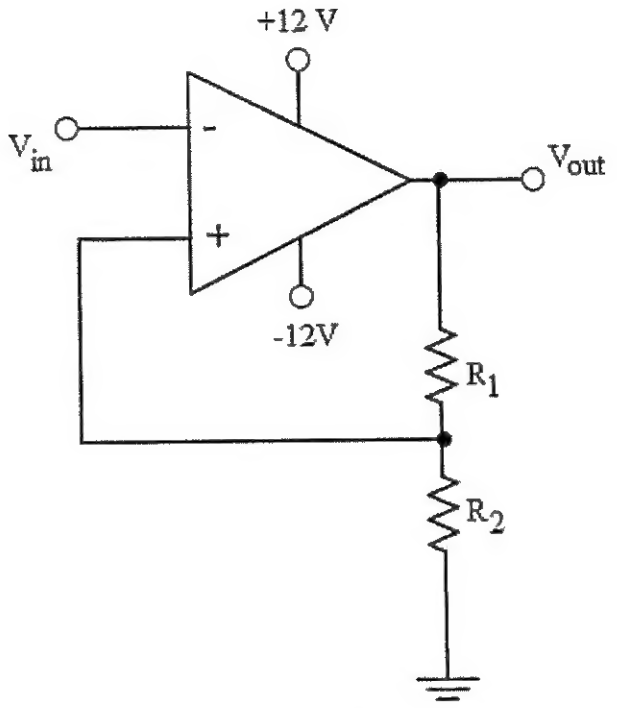

Fig. 4 (a)

(iii) Determine the upper triggering point (UTP) and lower triggering point (LTP) voltages of the circuit.

[1.5+1.5 marks]

(iv) Assuming an ideal op-amp, draw the Hysteresis curve of the circuit.

[4 marks]

Continued .....

(b) The circuit shown in Fig. Q4 (b) generates a triangular waveform at its output. The values are given as C = 0.05μF, R = R_1 = 10kΩ, +V_{cc} = 15V, -V_{EE} = -15V, R_F = 11.6 KΩ.

(i) Determine the capacitor voltage.

[2 marks]

(ii) What is the time period of the output waveform?

[3 marks]

(iii) Draw the transient response of the output voltage and capacitor voltage.

[4 marks]

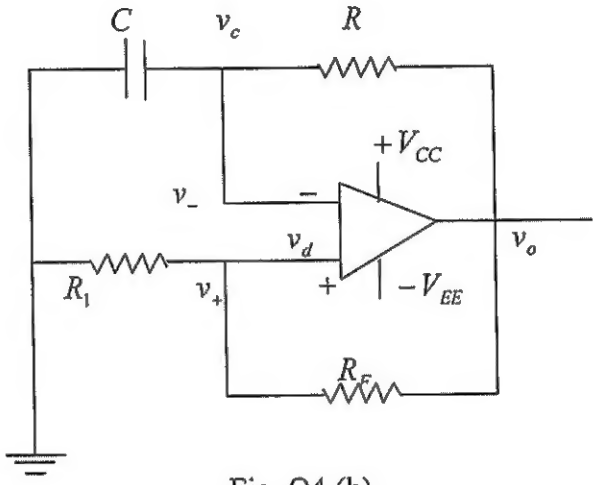

Fig. Q4 (b)

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